DWSUC3324PJ-Q ESD Protection Diode

Feature

- Bi-directional ESD protection of four I/O lines
- 33Watts peak pulse power (tp = 8/20μs)
- Working voltage: 3.3V
- Junction Capacitance: 0.13pF(Typ,Between I/O pins)
- Low clamping voltage
- Low leakage current
- AEC-Q101 qualified
- IEC 61000-4-2 ±15kV contact ±20kV air
- IEC 61000-4-5 (Lightning) 6A (8/20μs)

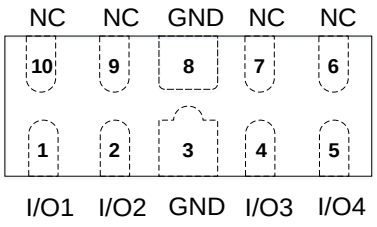
Application

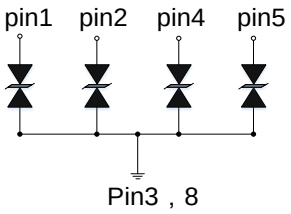
- USB2.0,USB3.0,USB3.1
- HDMI2.0,Displayport1.3,eSATA
- PCI Express
- Digital Display interface
- High speed serial interface

Mechanical Data

- Package: DFN2510-10L
- Molding compound flammability rating: UL 94V-0
- RoHS/WEEE Compliant

Schematic & PIN Configuration





Ordering Information

Part Number	Package	Marking	QTY per Reel	Reel Size
DWSUC3324PJ-Q	DFN2510-10L	324J	3000 pcs	7 inches

Absolute Maximum Rating (T_A=25°C unless otherwise Specified)

Parameter	Symbol	Value	Units
Peak Pulse Current (t_p =8/20μs)	I_{pp}	6	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±20 ±15	kV
Lead Soldering Temperature	T_L	260 (10seconds)	℃
Junction Temperature	T_J	-55 to + 150	℃
Storage Temperature	T_{stg}	-55 to + 150	℃

Electrical Characteristics (T_A=25°C unless otherwise Specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}				3.3	V
Reverse Leakage Current	I_R	V_{RWM}=3.3V,T=25℃			0.5	μA
Trigger Voltage	V_{BR}	I_T=1mA	5.0			V
Holding Voltage	V_H	I_H=100mA	2.0		3.3	V
ESD Clamping Voltage(1)	V_C	I_{TLP}=4A,tp=0.2/100ns		5.8		V
ESD Clamping Voltage(1)	V_C	I_{TLP}=16A,tp=0.2/100ns		9.4	11.8	V
ESD Dynamic Resistance(2)	R_{DYN}	T_{LP}=0.2/100ns		0.3	0.5	Ω
Clamping Voltage	V_C	I_{PP}=6A,t_p=8/20μs		5.5	6.5	V
Junction Capacitance	C_j	V_R = 1.65V, f = 1MHz Between I/O pins		0.13	0.18	pF
		V_R =1.65V, f = 1MHz I/O pin to GND		0.26	0.35	pF

Electrical Parameters (T_A = 25°C unless otherwise noted)

V_{RWM} ……Reverse Working Voltage Max.

I_R …… Maximum Reverse Leakage Current @ V_{RWM}

V_T…… Trigger Voltage

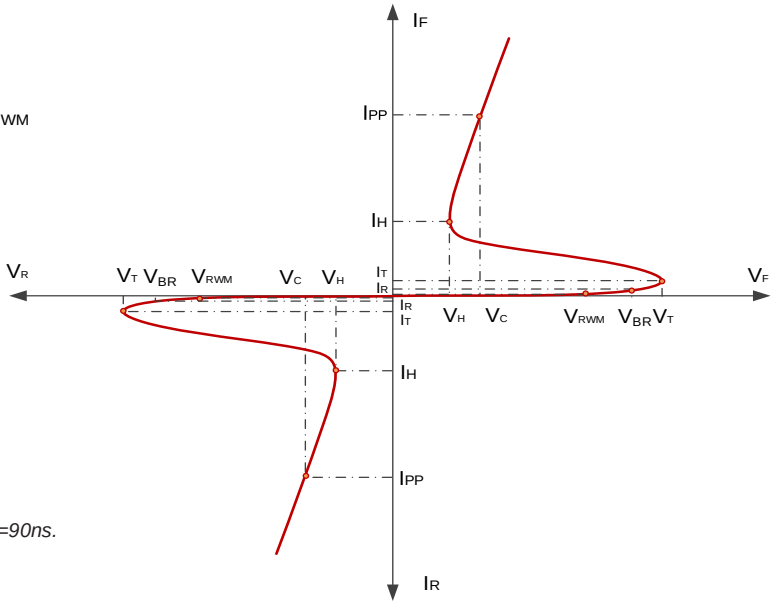
V_H…… Holding Voltage

I_H…… Holding Current

V_{BR} …… Reverse Breakdown Voltage

I_{PP} …… Maximum Reverse Peak Pulse Current

V_C …… Clamping Voltage @ I_{PP}



Note(1)：TLP Setting：I_{TLP} and V_{TLP} sample window:t1=70ns to t2=90ns.

Note(2)：Dynamic resistance calculated from I_{PP}=4A to I_{PP}=16A

Typical Characteristics

Figure1: Reverse Clamping Voltage vs. Peak Pulse Current

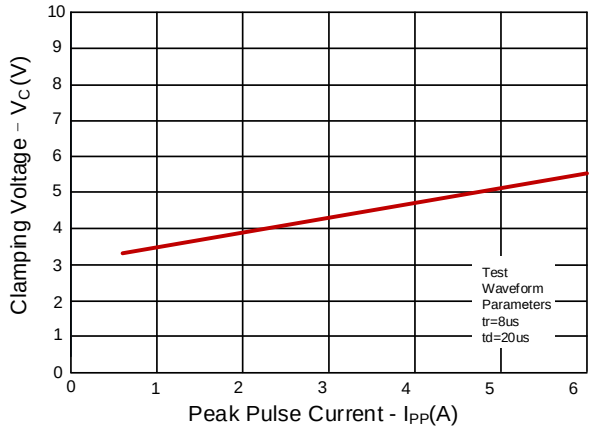


Figure 2: Power Derating Curve

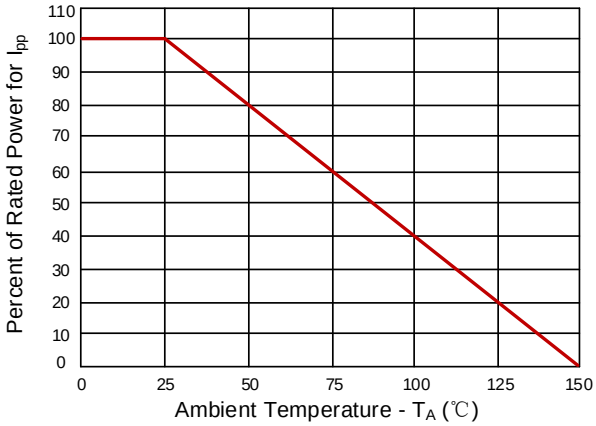


Figure3: TLP Positive I-V Curve

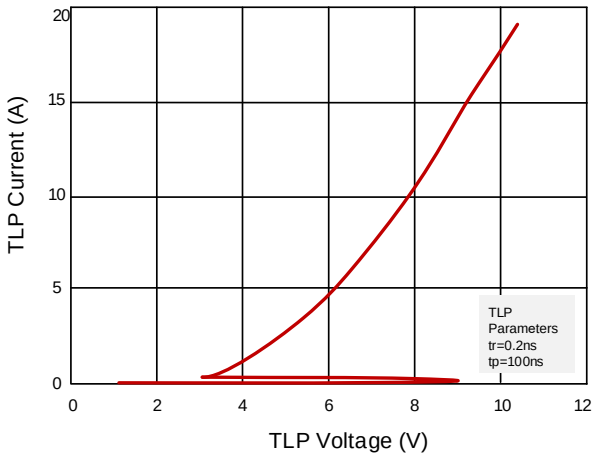


Figure4: TLP Negative I-V Curve

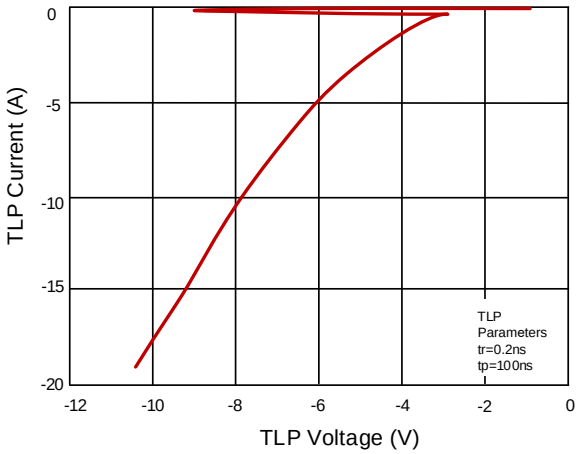


Figure5: IEC61000-4-2 : 8 kV positive pulse

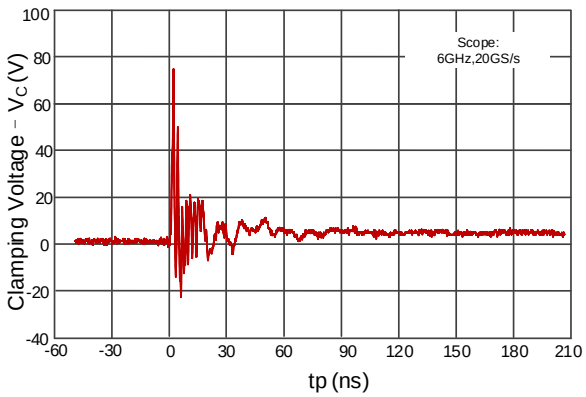
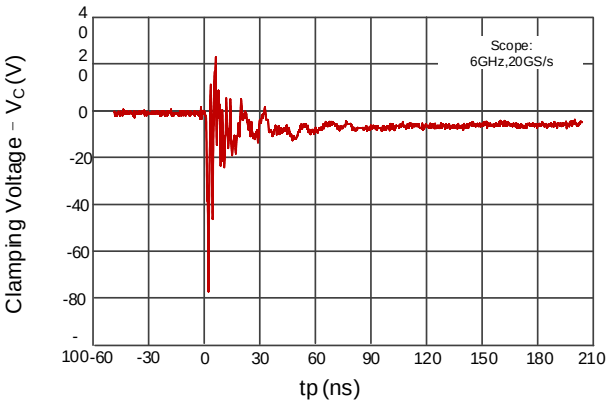
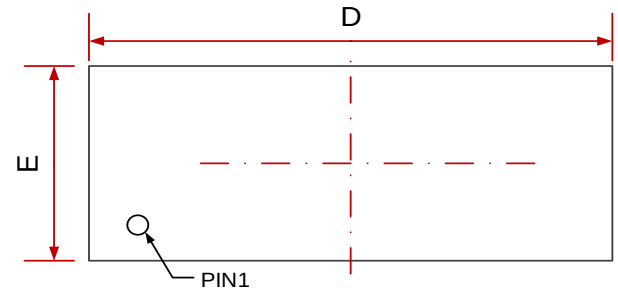


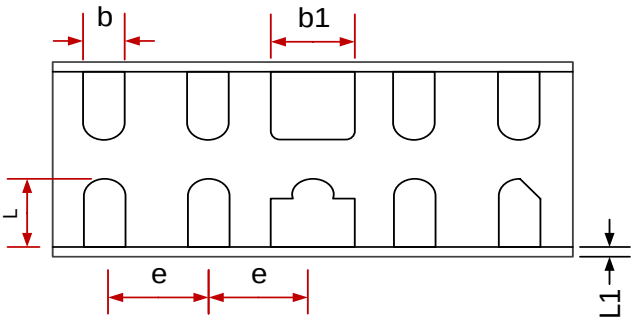
Figure6: IEC61000-4-2 : 8 Kv negative pulse



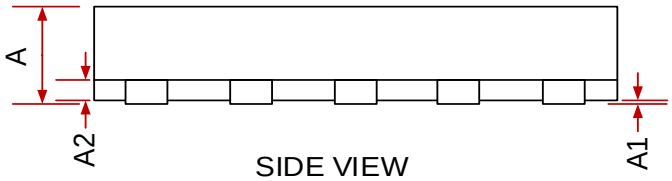
DFN2510-10L Outline Drawing



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Common Dimension (mm)			
PKG	DFN2510-10L		
REF.	MIN.	NOM.	MAX.
A	0.450	--	0.550
A1	--	--	0.005
A2	0.050	--	0.250
D	2.450	2.500	2.550
E	0.950	1.000	1.050
b	0.150	0.200	0.250
b1	0.350	0.400	0.450
L	0.300	0.350	0.400
L1	0.010	0.050	0.090
e	0.500BSC		